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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,208	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 5-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

- Claims 5-8 and 10 recite the limitation "further comprising the step of applying the voltage at a magnitude of equal to or greater than two times the operational supply voltage", which raises new matter. Nowhere in the specification describe or support such claimed limitation.

- Claims 9 and 11-12 recite the limitation "further comprising the step of preforming step b at an elevated temperature", which raises new matter. Nowhere in the specification describe or support such claimed limitation.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Mo et al. (U.S. Pat. No. 5,956,279).

Regarding claim 13, Mo et al. disclose a Static Random access memory device comprising: a test circuit (precharge circuit 200 conjunction with the burn-in current source circuit 300) integrated with the SRAM array; and connections that couple the test circuit to the SRAM array; wherein during probing (during wafer burn-in testing), the test circuit (precharge circuit 200 conjunction with the burn-in current source circuit 300) applies a voltage difference across a plurality of adjacent bitline pairs and/or wordline pairs of the SRAM array (col. 3, line 64 – col. 4, line 30; col. 5, lines 15-39); the voltage being larger than an operational supply voltage for the SRAM array (col. 1, lines 49-53), to thereby induce failure of metal stringers or defects (col. 1, lines 25-53; col. 2, lines 5-25; col. 3 line 64 – col. 4, line 29).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo et al. (U.S. Pat. 5,959,279).

Regarding claim 1, Mo et al. disclose a Static Random access memory device having a method for testing a semiconductor wafer, the semiconductor wafer having a plurality of die, comprising the steps of: (b) applying a voltage difference across a plurality of adjacent bitline

pairs **and/OR** wordline pairs of one **OR** more static random access memory (SRAM) arrays of at least one die of the semiconductor wafer, the voltage being larger than an operational supply voltage for the one **OR** more SRAM arrays, to thereby induce failure of metal stringers **OR** defects (precharge circuit 200 conjunction with the burn-in current source circuit 300 response to control signals to supply the test voltage to the device; col. 1, lines 25-53; col. 2, lines 5-25; col. 3 line 64 – col. 4, line30). Mo et al. do not specifically disclose the step (a) coupling an array of probes to the semiconductor wafer.

However, for wafer burn-in testing, it's known and obvious to one skill in the art that the memory device under test, must be probing to the test device in order to establish the communication between the test device and the device under test so that the test signals can supply to the device and the test result can send back to the tester to determine the condition of the device under test. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mo's device to include the limitation of the method to include the step (a) coupling an array of probes to the semiconductor wafer as a first step to establish the communication between the test device and the device under test prior the step supplying the test signals to the device and the test result can send back to the tester to determine the condition of the device under test.

Regarding claim 2, Mo et al. disclose all of the method steps of claim 1, further comprising the step of simultaneously applying the voltage across respective pairs of substantially all parallel bitline pairs **AND/OR** wordlines pairs of the one **OR** more SRAM arrays (col. 2, lines 54-61, col. 3, lines 20-31).

Regarding claim 3, Mo et al. disclose all of the method steps of claim 1, further comprising the step of simultaneously applying a voltage across respective pairs of substantially all parallel bitline pairs **AND/OR** wordlines pairs of the one **OR** more SRAM arrays of more that one die of the semiconductor wafer (col. 2, lines 64-61, col. 3, lines 20-31).

Regarding claim 4. Mo et al. disclose all of the method steps of claim 1, further comprising the step of applying the voltage across other adjacent, parallel metal lines (metal lines can be word-lines or bit-lines) of the one **OR** more SRAM arrays (col. 2, lines 54-61, col. 3, lines 20-31).

Regarding claim 5, as best understood, Mo et al. disclose all of the method steps of claim 1 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure as design choice.

Regarding claim 6, as best understood, Mo et al. disclose all of the method steps of claim 2 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the

word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure as design choice.

Regarding claim 7, Mo et al. disclose all of the method steps of claim 3 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation the of method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure as design choice.

Regarding claim 8, Mo et al. disclose all of the method steps of claim 4 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines

AND/OR bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure as design choice.

7. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo et al. (U.S.Pat. No. 5,956,279) in view of McClure (U.S.Pat. No. 5,619,462).

Regarding claim 9, Mo et al. disclose all of the method steps of claim 1 except for the step of preforming step b at an elevated temperature.

McClure discloses a circuit and method for fault detection for entire wafer stress test comprising the teaching placing the device under test into burn-in oven, elevating the device temperature and then applying the test voltage to the device to exercising the test so that the test time can be shorten and avoiding consequent burn-in of package (col. 1, lines 22-25; col. 2, lines 35-48). Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to include McClure's teaching into Mo's device to further disclose the limitation preforming step b at an elevated temperature so that the test time can be shorten and avoiding consequent burn-in of package.

Regarding claim 10, Mo et al. disclose all of the method steps of claim 9 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the

operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure as design choice.

Regarding claim 11, Mo et al. disclose all of the method steps of claim 3 except for the step of preforming step b at an elevated temperature.

McClure discloses a circuit and method for fault detection for entire wafer stress test comprising the teaching placing the device under test into burn-in oven, elevating the device temperature and then applying the test voltage to the device to exercising the test so that the test time can be shorten and avoiding consequent burn-in of package (col. 1, lines 22-25; col. 2, lines 35-48). Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to include McClure's teaching into Mo's device to further disclose the limitation preforming step b at an elevated temperature so that the test time can be shorten and avoiding consequent burn-in of package.

Regarding claim 12, Mo et al. disclose all of the method steps of claim 4 except for the step of preforming step b at an elevated temperature.

McClure discloses a circuit and method for fault detection for entire wafer stress test comprising the teaching placing the device under test into burn-in oven, elevating the device temperature and then applying the test voltage to the device to exercising the test so that the test time can be shorten and avoiding consequent burn-in of package (col. 1, lines 22-25; col. 2, lines 35-48). Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to include McClure's teaching into Mo's device to further disclose the limitation preforming step b at an elevated temperature so that the test time can be shorten and avoiding consequent burn-in of package.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
November 8, 2002

Gene N Auduong
Examiner
Art Unit 2818